

REMARKS

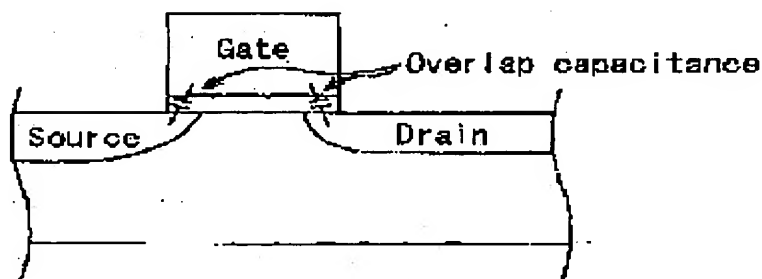
Claims 1-4, 6-10, 12-14, 16-19, 21-23, and 25-32 are pending. Claims 1-4, 6-10, 12-14, 16-19, 21-23, 25 and 26 are allowed. Claims 27 and 29 have been amended herein. New claims 31 and 32 have been added herein. Support for the amendment and new claims is detailed below.

Applicants Response to Claim Rejections under 35 U.S.C. §103(a)

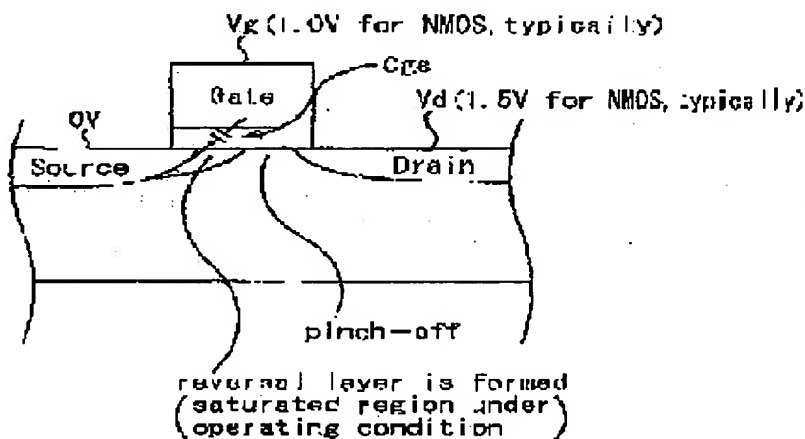
Claims 27 and 28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Talwar et al. (U.S. Patent No. 6,380,044) in view of Guegan (U. S. Patent No. 5,705,410) further in view of Zolper et al. (U.S. Patent No. 6,083,781); and, claims 29 and 30 stand rejected as being unpatentable over Talwar et al. (U.S. Patent No. 6,380,044) in view of Guegan (U. S. Patent No. 5,705,410) further in view Chou et al. (U.S. Patent No. 5,308,780) further in view of Zolper et al. (U.S. Patent No. 6,083,781). In response thereto, applicants have amended claims 27 and 29 to more distinctly claim the invention.

Specifically, applicants have included the capacitance between the gate and source is an overlap capacitance. The present application discloses that “the capacitance is an index showing the amount of overlap between the source and the drain and the gate electrode”, that is, a capacitance between the gate and the source indicates “an overlap capacitance.” See line 28 of page 36 to line 3 of page 37 of the specification. Applicants respectfully submit that the cited references do not teach or suggest an overlap capacitance.

As in the reference drawing below, the overlap capacitance is a capacitance in the region where the gate electrode and the source (drain) overlap one another. The present application discloses that the amount of overlap between the source and the drain and the gate electrode is $0.25(\text{fF}/\mu\text{m}/\text{side})$ or more



On the other hand, in *Zolper et al.*, a gate-to-source capacitance C_{gs} contains a capacitance between the gate electrode and the channel region having a reverse layer. As seen in the following figure.



Zolper fails to disclose that the source and drain are constituted by integrating a shallow junction and a deep junction, and further, **Zolper** fails to teach or show that the source and the drain and the gate electrode are overlapped. Therefore, the “capacitance” in **Zolper** is not the overlap capacitance of the present invention. Accordingly, applicants respectfully submit that the limitation of amended claims 27 and 29 is not taught or suggested by **Zolper**, and therefore the invention of the claims is not obvious.

The Office Action asserts that one of ordinary skill in the art would have combined the references “in order to have a semiconductor structure with increased performance.” Applicants respectfully submit that there is no disclosure in the cited references that would suggest or teach that the resulting combination would produce a structure with increased performance.

Applicants respectfully submit that one of ordinary skill in the art would not have combined the references. **Talwar et al.** does not disclose a shallow junction seeping under the gate, as acknowledged by the Office Action. One of ordinary skilled in the art would not have looked to the teachings of **Guegan** and been able to modify **Zolper et al.** such that the shallow extension (junction) would extend under the gate. The structure disclosed by **Guegan** is entirely different from **Talwar et al.** An object of **Guegan** is to provide an improved method for obtaining a high concentration doping of the channel as illustrated in Figs. 1 – 3. Figs. 1 – 3 of **Guegan** illustrate the admitted prior art of **Guegan**. The improved method of **Guegan** is illustrated in Figs. 4 – 6, wherein oblique implantation of ions is performed using masks 114 and 115. Subsequent to the oblique implantation, the gate is formed. It would not appear possible to

combine the teachings of **Guegan** with the teachings of **Talwar et al.** so as to obtain a shallow junction seeping into the single crystal semiconductor under said gate and a deep junction extending under said shallow junction.

Even if the teachings of **Talwar et al.** and **Guegan** could somehow be combined, the combination would not teach the claimed capacitance. The claimed capacitance is an index showing the amount of overlap between the source and the drain and the gate electrode (see, for example, page 18, lines 15 - 28). The capacitance disclosed by **Guegan** is a pn junction capacitance between the source and drain and the substrate.

The teachings of **Zolper et al.** does not provide the teachings which **Talwar et al.** and **Guegan** lack. As discussed above, **Zolper et al.** does not disclose a source and a drain constituted by integrating a shallow junction and a deep junction. Furthermore, **Zolper et al.** does not teach a shallow junction seeping into a single crystal semiconductor under the gate. Thus, the capacitance disclosed by **Zolper et al.** would not correspond to the claimed capacitance which is an index showing the amount of overlap between the source and the drain and the gate electrode.

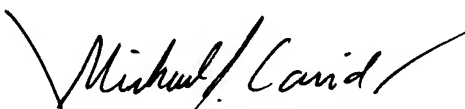
In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

Amendment under 37 C.F.R. §1.114
Serial No. 10/083,684
Attorney Docket No. 020254

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

A handwritten signature in black ink, appearing to read "Michael J. Caridi", with a large, sweeping flourish at the end.

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